REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add device type 02. Add package Y. Correct table I, I_{CC}. Editorial changes throughout.	92-01-16	Monica Poelking
B	Changes in accordance with NOR 5962-R058-94	93-12-02	Tim Noh
C	Changes in accordance with NOR 5962-R025-95	94-11-15	Thomas M. Hess
D	Add device 03. Editorial changes throughout.	95-09-26	Monica Poelking

REV																				
SHEET																				
REV	D	D	D	D	D	D	D	D	D	D	D									
SHEET	15	16	17	18	19	20	21	22	23	24	25									

REV STATUS OF SHEETS	REV	D	D	D	D	D	D	D	D	D	D	D	D	D
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

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DRAWING APPROVAL DATE
89-06-23

REVISION LEVEL
D

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUIT, DIGITAL, CMOS, 32-BIT DMA CONTROLLER WITH INTEGRATED SYSTEM SUPPORT PERIPHERALS, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**67268**	**5962-89593**

SHEET 1 OF 25

DESC FORM 193
JUL 94

5962-E258-95

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part or Identifying Number (PIN). The complete PIN shall be as shown in the following example:

5962-89593	01	X	X
Drawing number	Device type (see 1.2.1)	Case outline (see 1.2.2)	Lead finish (see 1.2.3)

1.2.1 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function	Frequency
01	82380	32-bit DMA controller with integrated system support peripherals	16 MHz
02	82380	32-bit DMA controller with integrated system support peripherals	20 MHz
03	82380	32-bit DMA controller with integrated system support peripherals	25 MHz

1.2.2 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
Y	See figure 1	164	Leaded chip carrier leads
Z	CMGA6-P132	132	Pin grid array package

1.2.3 Lead finish. The lead finish shall be as specified in MIL-STD-883 (see 3.1 herein). Finish letter "X" shall not be marked on the microcircuit or its packaging. The "X" designation is for use in specifications when lead finishes A, B, and C are considered acceptable and interchangeable without preference.

1.3 Absolute maximum ratings.

Storage temperature range	-65°C to +150°C
Voltage on any pin with respect to ground	-0.5 V dc to +6.5 V dc
Power dissipation (P_D)	2.0 W
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction-to-case (Θ_{JC}):	
Case Z	See MIL-STD-1835
Case Y	+8°C/W
Junction temperature (T_J)	+175°C

1.4 Recommended operating conditions.

Case operating temperature range (T_C)	-55°C to +125°C
Supply voltage range (V_{CC})	+4.75 V dc to +5.25 V dc

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and bulletin. Unless otherwise specified, the following specification, standards, and bulletin of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-I-38535 - Integrated Circuits (Microcircuits) Manufacturing, General Specification for.

STANDARDS

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-1835 - Microcircuit Case Outlines.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

(Copies of the specification, standards, and bulletin required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-I-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-I-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-I-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-STD-883 (see 3.1 herein) and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.2 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Functional block diagram. The functional block diagram shall be as specified on figure 3.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full (case or ambient) operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103 (see 6.6 herein).

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.6 herein). The certificate of compliance submitted to DESC-EC prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DESC-EC shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.9 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Input low voltage	V_{IL}		1,2,3	All	-0.3 1/	0.8	V
Input high voltage	V_{IH}		1,2,3		2.0	1/ V_{CC} +0.3	V
CLK2 input low voltage	V_{ILC}		1,2,3		-0.3 1/	0.8	V
CLK2 input high voltage	V_{IHC}		1,2,3		V_{CC}-0.8	V_{CC} +0.3 1/	V
Output low voltage	V_{OL}	I_{OL} = 4 mA: A_2-A_{31}, D_0-D_{31}, I_{OL} = 5 mA: all others	1,2,3			0.45	V
Output high voltage	V_{OH}	I_{OH} = -1 mA: A_2-A_{31}, D_0-D_{31}, I_{OH} = -0.9 mA: all others	1,2,3		2.4		V
Input leakage current	I_{LI}	All inputs except: $\overline{IRQ11}$- -IRQ23, EOP, TOUT2/IRQ3 DREQ4, $0 < V_{IN} < V_{CC}$	1,2,3		-15	+15	µA
Input leakage current	I_{LI1}	Inputs: $\overline{IRQ11}$ - $\overline{IRQ23}$ EOP, TOUT2/IRQ3, DREQ4 $0 < V_{IN} < V_{CC}$ 2/	1,2,3			-325	µA
Output leakage current	I_{L0}	$0 < V_{OUT} < V_{CC}$	1,2,3		-15	+15	µA
Supply current	I_{CC}	CLK2 = 32 MHz 3/	1,2,3	01		240	mA
		CLK2 = 40 MHz 3/		02		248	
		CLK2 = 50 Mhz		03		375	
Input capacitance	C_I	f = 1 MHz See 4.3.1c	4	All		12	pF
CLK2 input capacitance	C_{CLK}		4	All		20	pF
Functional tests		$4.75 V \le V_{CC} \le 5.25 V$ See 4.3.1d	7,8	All			

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $V_{CC} = 5\ V \pm 5\%$ unless otherwise specified	Group A subgroups	Device types	Limits Min	Limits Max	Unit
Operating frequency	f_{MAX}	See figure 4	9,10,11	01	4	16	MHz
				02	4	20	
CLK2 period time	t_1		9,10,11	01	31.25	125	ns
				02	25	125	
				03	20	125	
CLK2 high time	t_{2a}	Measured at 2.0 V See figure 4	9,10,11	01	9		ns
				02	8		
				03	7		
CLK2 high time 1/	t_{2b}	Measured at V_{CC} -0.8 V See figure 4	9,10,11	01	5		ns
				02	5		
				03	4		
CLK2 low time	t_{3a}	Measured at 2.0 V See figure 4	9,10,11	01	9		ns
				02	8		
				03	7		
CLK2 low time 1/	t_{3b}	Measured at 0.8 V See figure 4	9,10,11	01	7		ns
				02	6		
				03	4		
CLK2 fall time 1/	t_4	Measured from V_{CC} -0.8 V to 0.8 V, see figure 4	9,10,11	01		8	ns
				02		8	
				03		7	
CLK2 rise time 1/	t_5	Measured from 0.8 V to V_{CC} -0.8 V, see figure 4	9,10,11	01		8	ns
				02		8	
				03		7	
A_2-A_{31}, $\overline{BE_0}$ -$\overline{BE_3}$, $EDACK_0$-$EDACK_2$ valid delay	t_6	See figure 4	9,10,11	01	4	36	ns
				02	4	30	
				03	4	20	
A_2-A_{31}, $\overline{BE_0}$ -$\overline{BE_3}$, float delay 1/	t_7		9,10,11	01	4	40	ns
				02	4	32	
A_2-A_{31}, $\overline{BE_0}$ -$\overline{BE_3}$, setup times	t_8		9,10,11	All	6		ns
A_2-A_{31}, $\overline{BE_0}$ -$\overline{BE_3}$, hold time	t_9		9,10,11	All	4		ns
W/$\overline{R}$, M/$\overline{IO}$, D/$\overline{C}$ valid delay	t_{10}		9,10,11	01	6	33	ns
				02	6	28	
				03	4	20	
W/$\overline{R}$, M/$\overline{IO}$, D/$\overline{C}$ float 1/ delay	t_{11}		9,10,11	01	4	35	ns
				02	4	30	
				03	4	29	
W/$\overline{R}$, M/$\overline{IO}$, D/$\overline{C}$ setup	t_{12}		9,10,11	All	6		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $V_{CC} = 5\ V \pm 5\%$ unless otherwise specified	Group A subgroups	Device types	Limits Min	Limits Max	Unit
W/$\overline{R}$, M/$\overline{IO}$, D/$\overline{C}$ hold time	t_{13}	See figure 4	9,10,11	All	4		ns
$\overline{ADS}$ valid delay	t_{14}		9,10,11	01	6	33	ns
				02	6	28	
				03	4	19	
$\overline{ADS}$ float delay 1/	t_{15}		9,10,11	01	4	35	ns
				02	4	30	
				03	4	29	
ADS setup time	t_{16}		9,10,11	01	21		ns
				02	15		
				03	12		
$\overline{ADS}$ hold time	t_{17}		9,10,11	All	4		ns
Slave mode D_0-D_{31} read	t_{18}		9,10,11	01	3	46	ns
				02	4	46	
				03	4	31	
Slave mode D_0-D_{31} read float delay 1/	t_{19}		9,10,11	01	6	35	ns
				02	6	29	
				03	6	21	
Slave mode D_0-D_{31} write setup time	t_{20}		9,10,11	01	31		ns
				02	29		
				03	20		
Slave mode D_0-D_{31} write hold time	t_{21}		9,10,11	01	26		ns
				02	26		
				03	20		
Master mode D_0-D_{31} write valid delay	t_{22}		9,10,11	01	4	48	ns
				02	4	38	
				03	6	27	
Master mode D_0-D_{31} write float delay 1/	t_{23}		9,10,11	01	4	35	ns
				02	4	27	
				03	4	19	
Master mode D_0-D_{31} read setup time	t_{24}		9,10,11	01	11		ns
				02	11		
				03	7		
Master mode D_0-D_{31} read hold time	t_{25}		9,10,11	01	6		ns
				02	6		
				03	4		
$\overline{READY}$ setup time	t_{26}		9,10,11	01	21		ns
				02	12		
				03	9		
$\overline{READY}$ hold time	t_{27}		9,10,11	All	4		ns
WSC0-WSC1 setup time	t_{28}		9,10,11	All	6		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $V_{CC} = 5 V \pm 5\%$ unless otherwise specified	Group A subgroups	Device types	Limits Min	Limits Max	Unit
WSC0-WSC1 hold time	t_{29}	See figure 4	9,10,11	01	21		ns
				02	21		
				03	15		
RESET hold time	t_{30}		9,10,11	01	4		ns
				02	4		
				03	4		
RESET setup time	t_{31}		9,10,11	01	13		ns
				02	12		
				03	9		
$\overline{\text{READY0}}$ valid delay	t_{32}		9,10,11	01	4	31	ns
				02	4	28	
				03	3	21	
CPU reset delay	t_{33}		9,10,11	01	2	18	ns
				02	2	16	
				03	2	14	
Hold delay	t_{34}		9,10,11	01	5	33	ns
				02	5	30	
				03	4	22	
HLDA setup time	t_{35}		9,10,11	01	21		ns
				02	17		
				03	17		
HLDA hold time	t_{36}		9,10,11	01	6		ns
				02	6		
				03	4		
$\overline{\text{EOP}}$ setup time	t_{37a}		9,10,11	01	21		ns
				02	17		
				03	13		
$\overline{\text{EOP}}$ hold time	t_{38a}		9,10,11	All	4		ns
$\overline{\text{EOP}}$ setup time	t_{37b}		9,10,11	01	11		ns
				02	11		
				03	10		
$\overline{\text{EOP}}$ hold time	t_{38b}		9,10,11	01	11		ns
				02	11		
				03	10		
$\overline{\text{EOP}}$ valid delay	t_{39}		9,10,11	01	5	38	ns
				02	5	30	
				03	4	21	
$\overline{\text{EOP}}$ float delay 1/	t_{40}		9,10,11	01	5	40	ns
				02	5	32	
				03	4	21	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $V_{CC} = 5\ V \pm 5\%$ unless otherwise specified	Group A subgroups	Device types	Limits Min	Limits Max	Unit
DREQ setup time	t_{41a}	Synchronous See figure 4	9,10,11	01	21		ns
				02	19		
				03	17		
DREQ hold time	t_{42a}		9,10,11	All	4		ns
DREQ setup time	t_{41b}		9,10,11	01	11		ns
				02	11		
				03	4		
DREQ hold time	t_{42b}		9,10,11	01	11		ns
				02	11		
				03	10		
INT valid delay	t_{43}	See figure 4	9,10,11	All		500	ns
$\overline{NA}$ setup time	t_{44}	See figure 4	9,10,11	01	11		ns
				02	10		
				03	7		
$\overline{NA}$ hold time	t_{45}		9,10,11	01	15		ns
				02	15		
				03	8		
CLKIN frequency	t_{46}		9,10,11	All	0 1/	10	MHz
CLKIN high time	t_{47}	Measured at 2.0 V See figure 4	9,10,11	All	30		ns
CLKIN low time	t_{48}	Measured at 0.8 V See figure 4	9,10,11	All	50		ns
CLKIN rise time 1/	t_{49}	Measured from 0.8 V to V_{CC} -0.8 V, see figure 4	9,10,11	All		10	ns
CLKIN fall time 1/	t_{50}	Measured from V_{CC} -0.8 V to 0.8 V	9,10,11	All		10	ns
TOUT1/$\overline{REF}$ valid from CLK2	t_{51}	See figure 4 4/	9,10,11	01	4	36	ns
				02	4	30	
				03	4	20	
TOUT1/$\overline{REF}$ valid from CLKIN	t_{52}		9,10,11	01	3	93	ns
				02	3	93	
				03	3	90	
$\overline{TOUT2}$ valid delay	t_{53}		9,10,11	01	3	93	ns
				02	3	93	
				03	3	90	
$\overline{TOUT2}$ float delay	t_{54}		9,10,11	01	3	40	ns
				02	3	40	
				03	3	37	
$\overline{TOUT3}$ valid delay	t_{55}		9,10,11	01	3	93	ns
				02	3	93	
				03	3	90	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

1/ Guaranteed to the limit specified herein, if not tested.

2/ These pins should not be left floating.

3/ I_{CC} is specified with inputs driven to CMOS levels, and outputs driving CMOS loads. I_{CC} may be higher if inputs are driven to TTL levels, or if outputs are driving TTL loads.

4/ All outputs loaded to 50 pf.

Case Y

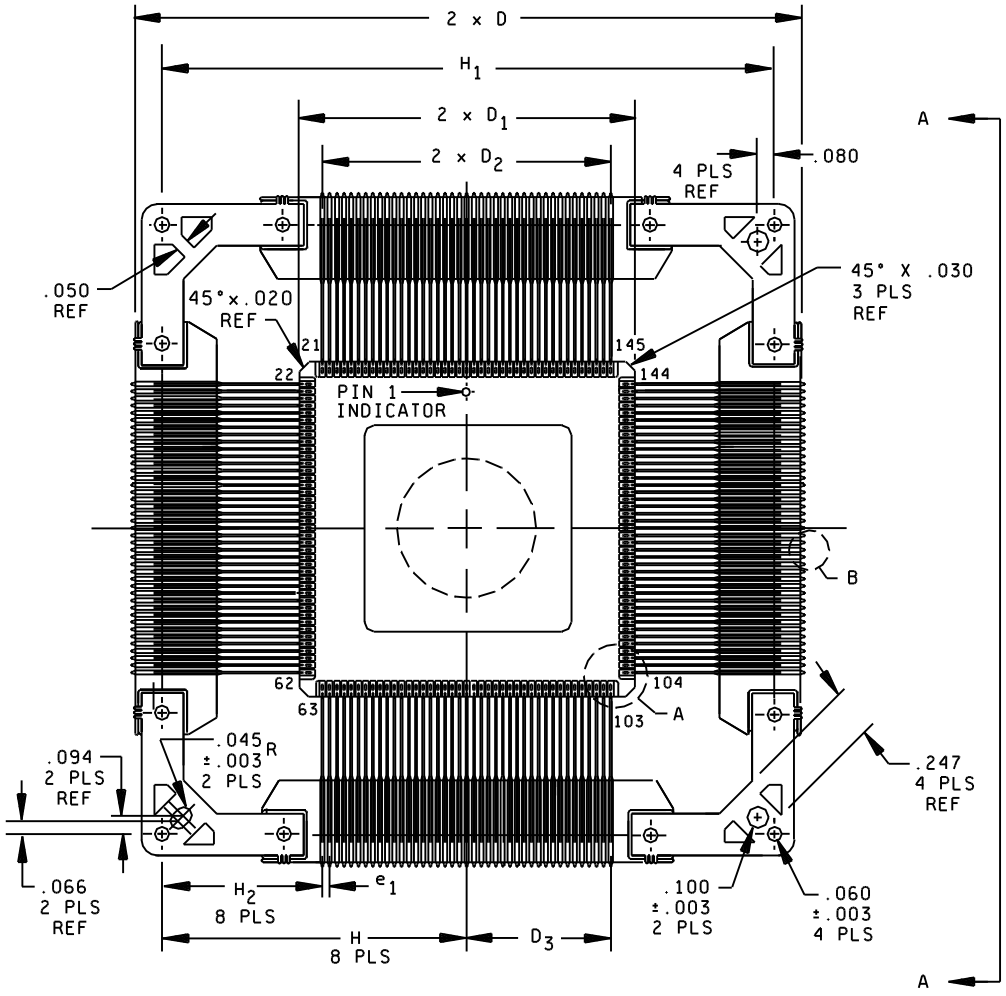
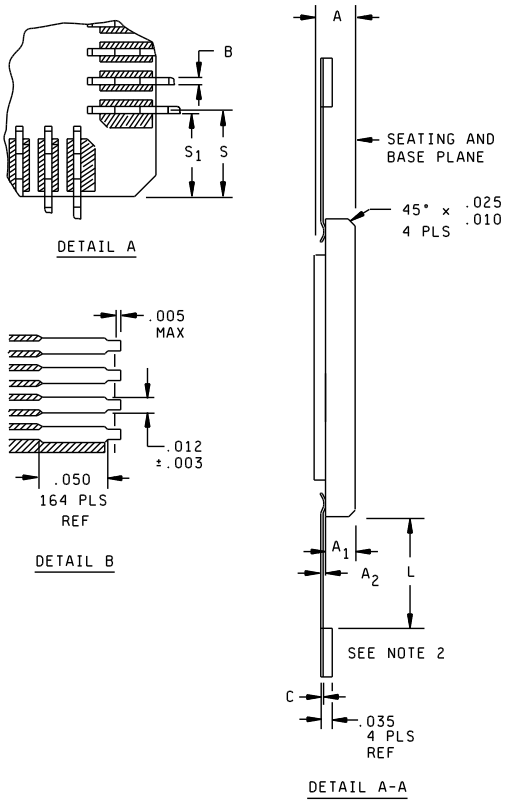


FIGURE 1. Case outline.

Case Y



Symbol	Inches		Millimeters	
	Min	Max	Min	Max
A	.088	.115	2.23	2.92
A_1	.078	.094	1.98	2.39
A_2	.006	.012	0.15	0.30
B	.007	.010	0.18	0.25
C	.004	.006	0.10	0.15
D	2.480	2.520	63.00	64.01
D_1	1.120	1.140	28.45	28.96
D_2	1.00 BASIC		25.40 BASIC	
D_3	.500 BASIC		12.70 BASIC	
e_1	.023	.027	0.58	0.69
H	1.150 BASIC		29.21 BASIC	
H_1	2.30 BASIC		58.42 BASIC	
H_2	.650 BASIC		16.51 BASIC	
L	.365	.395	9.27	10.03
N	164 TERMINALS			
S	.060	.080	1.52	2.03
S_1	.060	.076	1.52	1.93

NOTES:
1. Dimensions are in inches.
2. Metric equivalents are given for general information only.
3. Symbols B and C dimensions shall be increased by .002 inch when solder coat is added.

FIGURE 1. Case outline - Continued.

Case Y

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	A_4	28	A_{22}	55	D_{13}	82	D_1
2	V_{CC}	29	V_{SS}	56	D_5	83	D_{24}
3	V_{SS}	30	V_{CC}	57	D_{28}	84	D_{16}
4	A_5	31	A_{23}	58	D_{20}	85	D_8
5	A_6	32	A_{24}	59	D_{12}	86	D_0
6	A_7	33	A_{25}	60	V_{CC}	87	V_{SS}
7	A_8	34	A_{26}	61	V_{SS}	88	V_{CC}
8	A_9	35	A_{27}	62	NC	89	$\overline{\text{READY0}}$
9	V_{CC}	36	A_{28}	63	NC	90	TOUT1/$\overline{\text{REF}}$
10	V_{SS}	37	A_{29}	64	V_{CC}	91	HOLD
11	A_{10}	38	A_{30}	65	D_4	92	M/$\overline{\text{TO}}$
12	A_{11}	39	A_{31}	66	D_{27}	93	V_{SS}
13	A_{12}	40	NC	67	D_{19}	94	V_{CC}
14	A_{13}	41	D_{31}	68	D_{11}	95	NC
15	V_{CC}	42	D_{23}	69	D_3	96	NC
16	V_{SS}	43	D_{15}	70	D_{26}	97	W/$\overline{\text{R}}$
17	A_{14}	44	D_7	71	D_{18}	98	D/$\overline{\text{C}}$
18	A_{15}	45	D_{30}	72	D_{10}	99	$\overline{\text{TOUT3}}$
19	A_{16}	46	V_{SS}	73	D_2	100	$\overline{\text{TOUT2}}$/$\overline{\text{TRQ3}}$
20	A_{17}	47	V_{CC}	74	V_{SS}	101	CPURST
21	NC	48	D_{22}	75	V_{CC}	102	NC
22	NC	49	D_{14}	76	D_{25}	103	V_{CC}
23	V_{CC}	50	D_6	77	D_{17}	104	V_{SS}
24	A_{18}	51	V_{SS}	78	D_9	105	V_{CC}
25	A_{19}	52	V_{CC}	79	V_{SS}	106	NC
26	A_{20}	53	D_{29}	80	CLK2	107	V_{SS}
27	A_{21}	54	D_{21}	81	V_{SS}	108	V_{CC}

FIGURE 2. Terminal connections.

Case Y

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
109	$\overline{\text{READY}}$	123	$\overline{\text{TRQ18}}$	137	$\overline{\text{NA}}$	151	EDACK1
110	RESET	124	$\overline{\text{TRQ19}}$	138	DREQ6	152	EDACK2
111	WSC1	125	$\overline{\text{TRQ20}}$	139	DREQ7	153	V_{CC}
112	WSC0	126	$\overline{\text{TRQ2}}$	140	V_{CC}	154	V_{SS}
113	V_{SS}	127	$\overline{\text{TRQ2}}$	141	V_{SS}	155	$\overline{\text{EOP}}$
114	CLKIN	128	$\overline{\text{TRQ2}}$	142	NC	156	$\overline{\text{ADS}}$
115	V_{CC}	129	V_{CC}	143	NC	157	$\overline{\text{BE}}_0$
116	$\overline{\text{TRQ11}}$	130	V_{SS}	144	NC	158	$\overline{\text{BE}}_1$
117	$\overline{\text{TRQ12}}$	131	DREQ0	145	NC	159	$\overline{\text{BE}}_2$
118	$\overline{\text{TRQ13}}$	132	DREQ1	146	HLDA	160	$\overline{\text{BE}}_3$
119	$\overline{\text{TRQ14}}$	133	DREQ2	147	INT	161	V_{CC}
120	$\overline{\text{TRQ15}}$	134	DREQ3	148	NC	162	V_{SS}
121	$\overline{\text{TRQ16}}$	135	DREQ4/$\overline{\text{TRQ9}}$	149	NC	163	A_2
122	$\overline{\text{TRQ17}}$	136	DREQ5	150	EDACK0	164	A_3

FIGURE 2. Terminal connections - Continued.

Case Z

Pin/signal		Pin/signal		Pin/signal		Pin/signal	
A7	A_{31}	A8	D_{31}	P12	V_{CC}	L14	V_{SS}
C7	A_{30}	B9	D_{30}	M14	V_{CC}	A1	V_{SS}
B7	A_{29}	A11	D_{29}	P1	V_{CC}	P13	V_{SS}
A6	A_{28}	C11	D_{28}	P2	V_{CC}	N1	V_{SS}
B6	A_{27}	D12	D_{27}	P14	V_{CC}	N2	V_{SS}
C6	A_{26}	E13	D_{26}	D1	V_{CC}	C1	V_{SS}
A5	A_{25}	F14	D_{25}	C14	V_{CC}	A3	V_{SS}
B5	A_{24}	J13	D_{24}	B1	V_{CC}	B14	V_{SS}
C5	A_{23}	B8	D_{23}	A2	V_{CC}	A13	V_{SS}
B4	A_{22}	C9	D_{22}	A4	V_{CC}	N14	V_{SS}
B3	A_{21}	B11	D_{21}	A12	V_{CC}	P6	IRQ23
C4	A_{20}	B13	D_{20}	A14	V_{CC}	N6	IRQ22
B2	A_{19}	D13	D_{19}	G14	CLK2	M7	IRQ21
C3	A_{18}	E14	D_{18}	L12	D/$\overline{C}$	N7	IRQ20
C2	A_{17}	G12	D_{17}	K12	W/$\overline{R}$	P7	IRQ19
D3	A_{16}	H13	D_{16}	L13	M/$\overline{IO}$	P8	IRQ18
D2	A_{15}	C8	D_{15}	K2	$\overline{ADS}$	M8	IRQ17
E3	A_{14}	A10	D_{14}	N4	$\overline{NA}$	N8	IRQ16
E2	A_{13}	C10	D_{13}	J12	HOLD	P9	IRQ15
E1	A_{12}	C12	D_{12}	M3	HLDA	N9	IRQ14
F3	A_{11}	D14	D_{11}	M6	DREQ0	M9	IRQ13
F2	A_{10}	F12	D_{10}	P5	DREQ1	N10	IRQ12
F1	A_9	G13	D_9	N5	DREQ2	P10	IRQ11
G1	A_8	K14	D_8	P4	DREQ3	M2	INT
G2	A_7	A9	D_7	M5	DREQ4/$\overline{IRQ9}$	N11	CLKIN
G3	A_6	B10	D_6	P3	DREQ5	K13	TOUT1/$\overline{REF}$
H1	A5	B12	D5	M4	DREQ6	N13	$\overline{TOUT2}$/$\overline{IRQ3}$
H2	A_4	C13	D_4	N3	DREQ7	M13	$\overline{TOUT3}$
J1	A_3	E12	D_3	K3	$\overline{EOP}$	M11	$\overline{READY}$
H3	A_2	F13	D_2	L3	EDACK0	H12	$\overline{READY0}$
J2	$\overline{BE}_3$	H14	D_1	M1	EDACK1	P11	WSC0
J3	$\overline{BE}_2$	J14	D_0	L2	EDACK2	M10	WSC1
K1	$\overline{BE}_1$	N12	RESET				
L1	$\overline{BE}_0$	M12	CPURST				

FIGURE 2. Terminal connections - Continued.

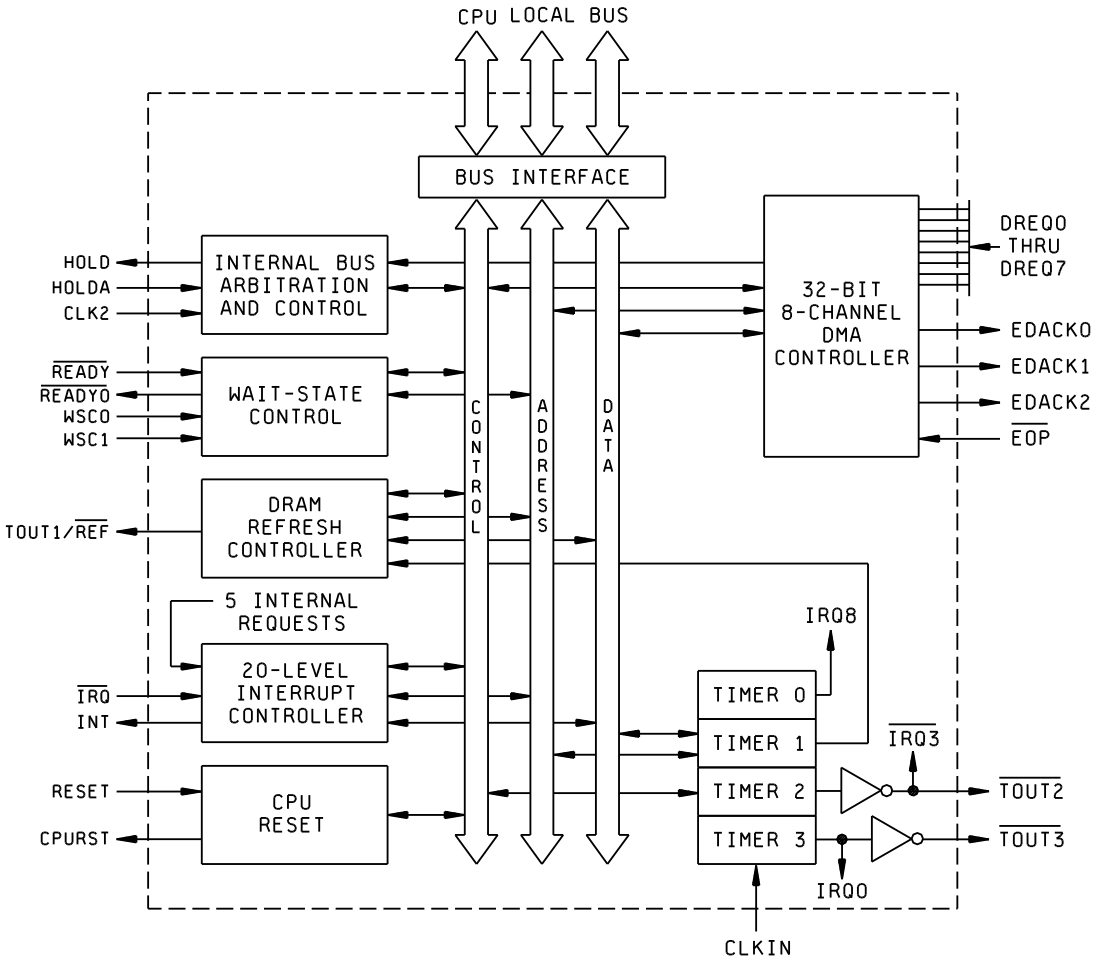
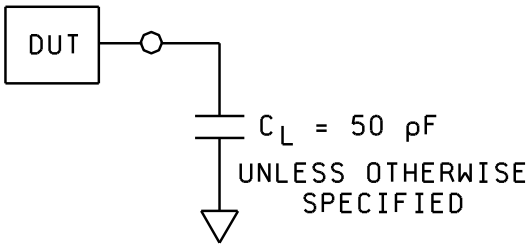
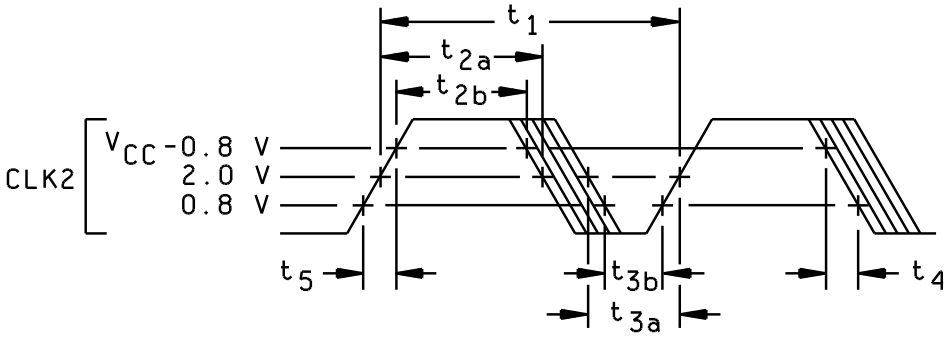


FIGURE 3. Functional block diagram.



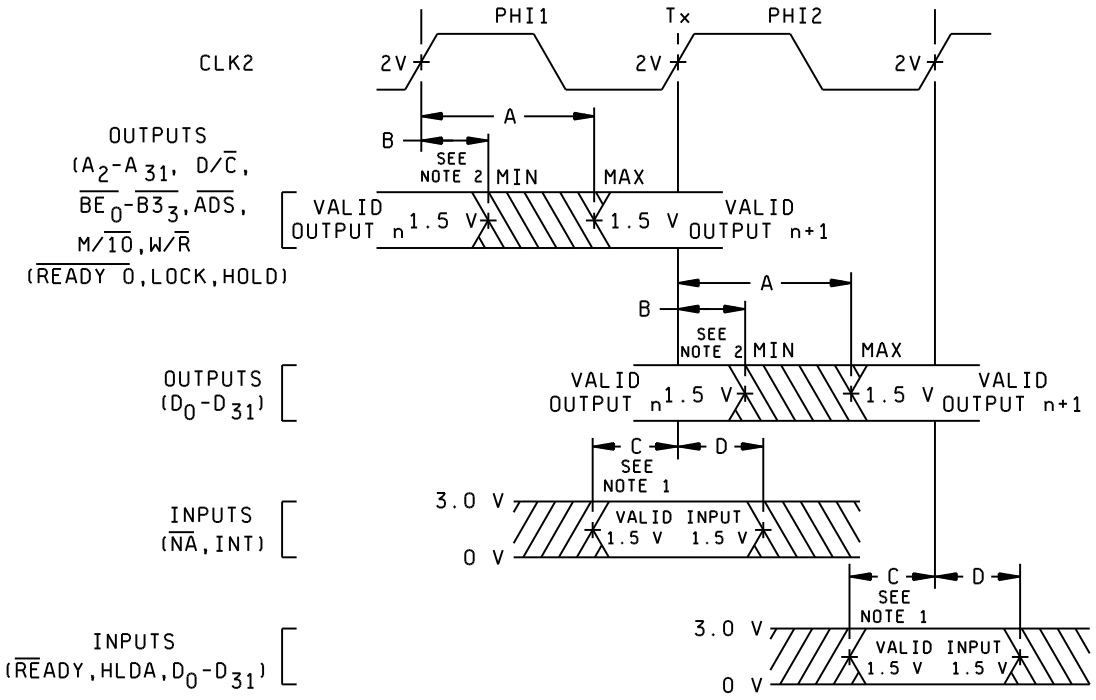
AC TEST CIRCUIT



CLK2 TIMING

NOTE: All ac timings are tested at 1.5 V threshold, unless otherwise specified.

FIGURE 4. AC test circuit and timing waveforms.

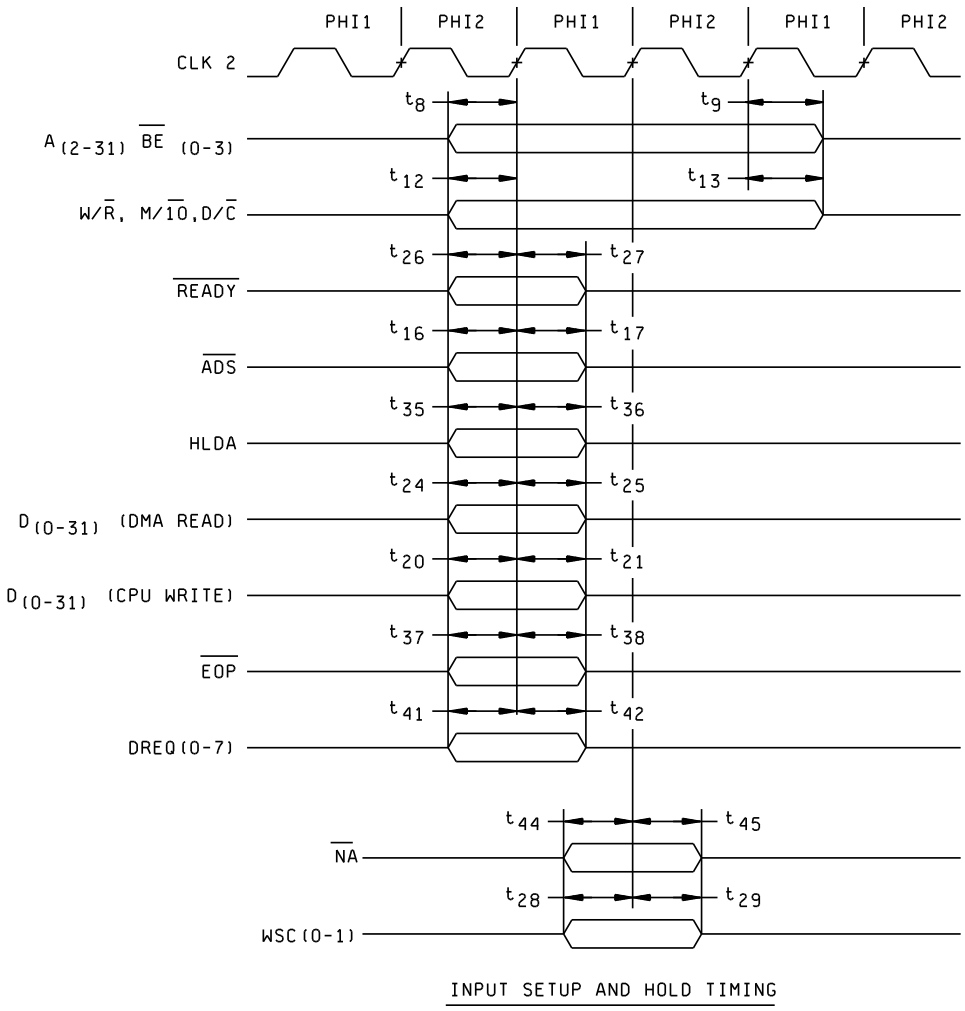


LEGEND:
- A - Maximum output delay specification.
- B - Minimum output delay specification.
- C - Minimum input setup specification.
- D - Minimum input hold specification.

NOTES:
1. Input waveforms have $t_r \leq 2$ ns from 0.8 V to 2 V.
2. Under rated loading (120 pF): output t_r, t_f is typically ≤ 4 ns from 0.8 V to 2 V.
3. All timing measurements are tested at 1.5 V, unless otherwise specified.

Drive levels and measurements points for ac specification.

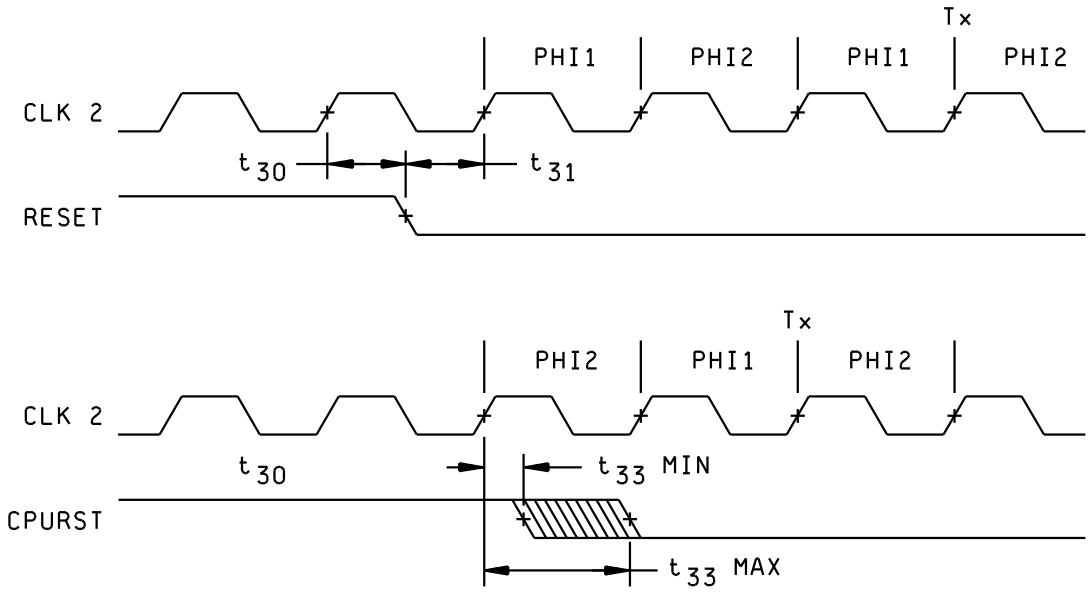
FIGURE 4. AC test circuit and timing waveforms - Continued.



INPUT SETUP AND HOLD TIMING

NOTE: All timing measurements are tested at 1.5 V, unless otherwise specified.

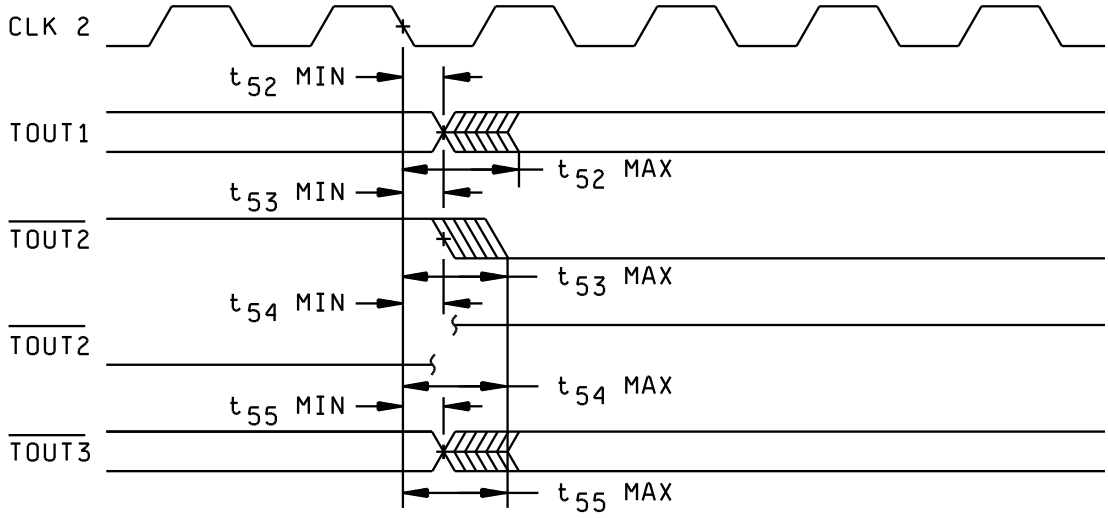
FIGURE 4. AC test circuit and timing waveforms - Continued.



RESET TIMING

NOTE: All timing measurements are tested at 1.5 V, unless otherwise specified.

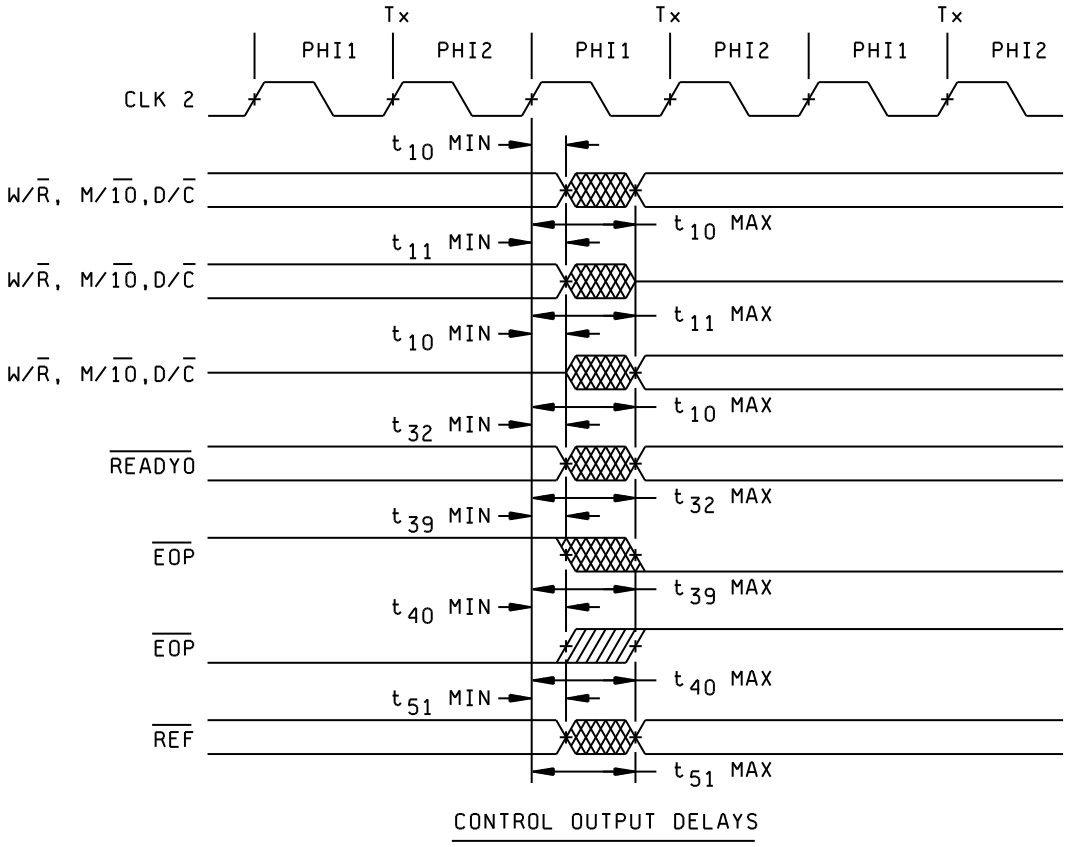
FIGURE 4. AC test circuit and timing waveforms - Continued.



TIMER OUTPUT DELAYS

NOTE: All timing measurements are tested at 1.5 V, unless otherwise specified.

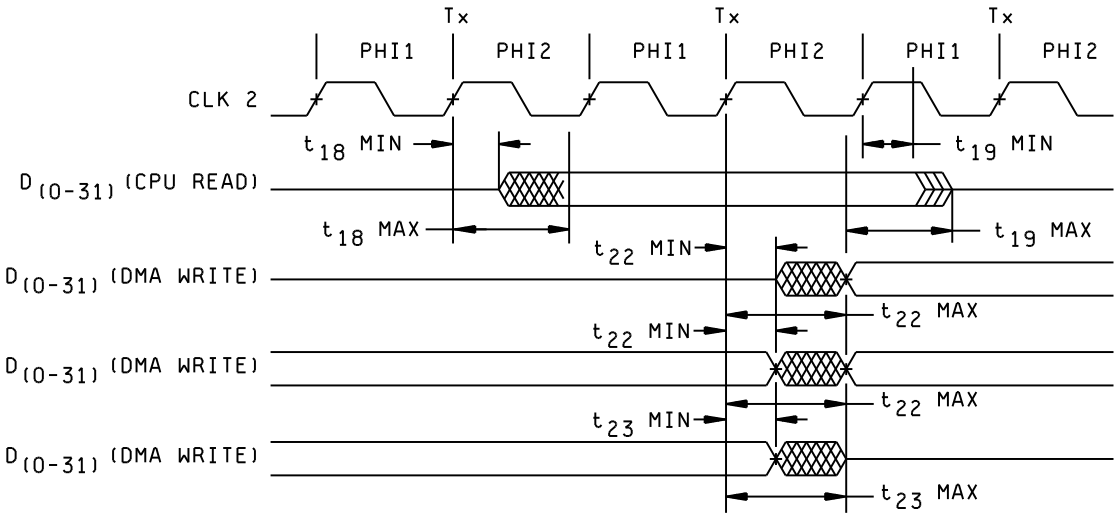
FIGURE 4. AC test circuit and timing waveforms - Continued.



CONTROL OUTPUT DELAYS

NOTE: All timing measurements are tested at 1.5 V, unless otherwise specified.

FIGURE 4. AC test circuit and timing waveforms - Continued.



DATA BUS OUTPUT DELAYS

NOTE: All timing measurements are tested at 1.5 V, unless otherwise specified.

FIGURE 4. AC test circuit and timing waveforms - Continued.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

(2) T_A = +125° C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with method 5005, table I)
Interim electrical parameters (method 5004)	
Final electrical test parameters (method 5004)	1*, 2, 3, 7*, 8, 9, 10, 11
Group A test requirements (method 5005)	1*, 2, 3, 7*, 8, 9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	2, 8a, 10

* PDA applies to subgroup 1.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} and C_{CLK} measurement) shall be measured only for the initial test and after process or design changes which may affect input capacitance.

d. Subgroups 7 and 8 shall include verification of the functionality of the device. These tests form a part of the manufacturer's test tape and shall be maintained and available from the approved source of supply.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-STD-883 (see 3.1 herein).

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal .

6.4 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and the applicable SMD. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DESC-EC, telephone (513) 296-6047.

6.5 Comments. Comments on this drawing should be directed to DESC-EC, Dayton, Ohio 45444-5270, or telephone (513) 296-5377.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-EC.

6.7 Pin descriptions.

Pin name	I/O	Description
A_0-A_{31}	I/O	Address bus. This is the 32-bit address bus. The addresses are doubleword memory and I/O addresses. These are three-state signals which are active active only during master mode. The address lines should be connected directly to the CPU's local bus.
D_0-D_{31}	I/O	Data bus. This is the 32-bit data bus. These pins are active outputs during interrupt acknowledges, during slave accesses, and when the device is in the master mode.
CLK2	I	Processor clock. This pin must be connected to CLK2. The device monitors the phase of this clock in order to remain synchronized with the CPU. This clock drives all of the internal synchronous circuitry.
$D/\overline{C}$	I/O	Data/control. $D/\overline{C}$ is used to distinguish between CPU control cycles and DMA or CPU data access cycles. It is active as an output only in the master mode.

Pin name	I/O	Description - Continued.
$\overline{BE}_0$	I/O	Byte enable 0. BE_0 active indicates that data bits D_0-D_7 are being accessed are being accessed or are valid. It is connected directly to the CPU's BE_0. The byte enable signals are active outputs when the device is in the master master mode.
$\overline{BE}_1$	I/O	Byte enable 1. $\overline{BE}_1$ active indicates that data bits D_8-D_{15} are being accessed or are valid. It is connected directly to the CPU's $\overline{BE}_1$. The byte enable signals are active only when the device is in the master mode.
$\overline{BE}_2$	I/O	Byte enable 2. $\overline{BE}_2$ active indicates that data bits D_{15}-D_{23} are being accessed or are valid. It is connected directly to the CPU's $\overline{BE}_2$. The byte enable signals are active only when the device is in the master mode.
$\overline{BE}_3$	I/O	Byte enable 3. $\overline{BE}_3$ active indicates that data bits D_{24}-D_{31} are being accessed or are valid. The byte enable signals are active only when the device is in the master mode. This pin should be connected directly to the CPU's $\overline{BE}_3$. This pin is used for factory testing and must be low during reset. The CPU drivers $\overline{BE}_3$ low during reset.
HOLD	0	Hold request. This is an active-high signal to the CPU to request control of the system bus. When control is granted, the CPU activates the hold acknowledge signal (HLDA).
HLDA	I	Hold acknowledge. This input signals tells the DMA controller that the CPU has relinquished control of the system bus to the DMA controller.

STANDARDIZED MILITARY DRAWING SOURCE APPROVAL BULLETIN

DATE: 95-09-26

Approved sources of supply for SMD 5962-89593 are listed below for immediate acquisition only and shall be added to MIL-BUL-103 during the next revision. MIL-BUL-103 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DESC-EC. This bulletin is superseded by the next dated revision of MIL-BUL-103.

Standardized military drawing PIN	Vendor CAGE number	Vendor similar PIN 1/
5962-8959301YX	34649	MQ82380-16/Q
5962-8959301ZX	34649	MG82380-16/Q
5962-8959302YX	34649	MQ82380-20/Q
5962-8959302ZX	34649	MG82380-20/Q
5962-8959303YX	34649	MQ82380-25/Q
5962-8959303ZX	34649	MG82380-25/Q

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
34649	Intel Corporation 3065 Bowers Ave. Santa Clara, CA 95051 Point of contact: 5800 W. Chandler Blvd. Chandler, AZ 85226